

REMARKS

The rejection of claim 1 under 35 U.S.C. § 103(a) is maintained. Claim 1 stands rejected over Ribner et al. (U.S. Patent No. 6,028,891, hereinafter Ribner).

Claim 1 calls for an asymmetric digital subscriber loop (ADSL) modem that includes an integrated circuit comprising an analog-to-digital converter to produce data at a relatively higher data rate. To reduce the higher data rate from the analog-to-digital converter to a lower data rate, the integrated circuit includes a device coupled to the analog-to-digital converter. The integrated circuit further includes a multiplexer which multiplexes the lower data rate and control information and transmits the data and control information externally of the integrated circuit. Reconsideration of the Section 103 rejection of claim 1 is respectfully requested since the Ribner reference does not render claim 1 obvious.

In particular, Ribner does not teach or suggest an integrated circuit with use of a multiplexer to multiplex the lower data rate and control information, as claimed in claim 1. Just because a circuit can conceivably be implemented as an integrated circuit does not necessarily mean that the asymmetric digital subscriber loop modem of claim 1 is taught or suggested to be implemented as an integrated circuit in the Ribner reference, especially absent any indication or teaching whatsoever as to an integrated circuit design. As typically recognized by a person of ordinary skill in the art of integrated circuits, certain characteristics or attributes of a circuit to be implemented as an integrated circuit must be fulfilled to some reasonable level prior to implementation thereof as an integrated circuit, depending upon a particular process in which the integrated circuit may be fabricated.

The Examiner asserts that the data on lines 95₀-95₃₁, combined by the Q.A.M. decoder 94, produces a properly arranged stream of data on line 90. Hence, from 32 input lines of data, the Q.A.M. decoder 94 decodes and combines them into a properly arranged stream of data, making it obvious that the Q.A.M. decoder 94 performs the function of a multiplexer to multiplex digital signals and control information as teaching a multiplexer that multiplexes the lower data rate data and control the information and transmit the data and control information externally of the integrated circuit.

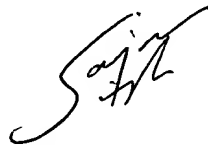
Rather, Ribner merely teaches that an FFT transformer and a line decoder may be implemented instead of a multiplexer as claimed in claim 1. Absent a teaching of a multiplexer

in combination with a device for an asymmetric digital subscriber loop (ADSL) modem of claim 1, the Examiner fails to show that the Ribner reference renders claim 1 obvious. The mere fact that a circuit can be implemented as an integrated circuit or a circuit may be devised for multiplexing is not sufficient to establish a *prima facie* case of obviousness, missing a specific teaching or suggestion as to a way to desirably implement that circuit. M.P.E.P. § 2143.01. Therefore, for at least this reason alone, the Examiner fails to establish a *prima facie* case of obviousness for claim 1. The dependent claims from claim 1 are also in condition for allowance for the reason that they depend from an allowable claim.

Claim 14 stands rejected under 35 U.S.C. § 103(a) over the Ribner reference. Based on the same analysis as set forth above in the context of claim 1, the Applicants respectfully submit to the Examiner that claim 14 limitations as a whole are not rendered obvious to one of ordinary skill in the relevant art. Accordingly, independent claim 14 and claims depending therefrom are patentably distinguishable over the Ribner reference. Pursuant to M.P.E.P. rules, the Examiner is respectfully requested to cite a reference for each instance where a notice for being something is well known in the art was taken. The Examiner is respectfully requested to reconsider the rejections of all pending claims.

In view of these remarks, the application is now in condition for allowance and the Examiner's prompt action in accordance therewith is respectfully requested.

Respectfully submitted,



Date: October 7, 2003

Sanjeev K. Singh under 37 C.F.R. § 10.9(b)
Registration No. 28,994
TROP, PRUNER & HU, P.C.
8554 Katy Freeway, Suite 100
Houston, Texas 77024
(713) 468-8880 [Phone]
(713) 468-8883 [Fax]